TITLE OF THE INVENTION:

RECTIFIERS AND RECTIFYING METHODS FOR USE IN TELECOMMUNICATIONS DEVICES

BACKGROUND OF THE INVENTION:

Field of the Invention:

[0001] Certain embodiments of the present invention are directed generally to rectifiers that may be included in electronic circuits in telecommunications devices. Certain other embodiments of the present invention are directed at methods of operating telecommunications with such rectifiers.

Description of the Related Art:

[0002] Rectifiers, which are typically used to transform alternating currents (AC) into direct currents (DC), are commonly included in the circuitry of telecommunications devices. More specifically, when included in a telecommunications device, rectifiers are commonly used to transform the AC component of signals received by the device, which typically take the form of radio frequency (RF) signals having a voltage component, into DC signals that may more easily be processed within the device. Examples of telecommunication device circuits where rectifiers are commonly included are Received Signal Strength Indicator (RSSI) and/or Transmitted Signal Strength Indicator (TSSI) circuits.

[0003] Figure 1 illustrates a schematic representation of a rectifier configuration according to the related art. The rectifier configuration schematically represented in Figure 1 may be found in RSSI circuits, TSSI circuits, or other circuits commonly found in telecommunications devices.

[0004] In operation, the rectifier configuration illustrated in Figure 1 receives the AC component of a signal received by the telecommunications device that includes the configuration. The AC component of the received signal enters the configuration through signal inputs 100 and is rectified

using asymmetric switching pair of rectifiers 110. Once rectified, the information in the AC component is output from the configuration as a DC signal through signal output 120. The DC signal output from signal output 120 is then further processed in the circuit that includes the configuration illustrated in Figure 1.

[0005] It should be noted that the rectifier configuration illustrated in Figure 1 is appropriately biased using biasing circuitry 130, which is operably connected to asymmetric switching pair 110. How much biasing circuitry 130 biases the rectifier configuration is dependent on the particulars of the system in which the rectifier configuration is included.

[0006] Also illustrated in Figure 1 is current mirror 140, which is operably connected between asymmetric switching pair 110 and signal output 120. Current mirror 140 regulates the amount of current that flows to signal output 120, and thereby promotes proper operation of the rectifier configuration.

[0007] Power supply voltage 150 is operably connected to asymmetric switching pair 110 in order to allow signals output from signal output 120 to compensate for fluctuations in the power supply voltage 150 over time. However, as illustrated in Figure 1, power supply voltage 150 is operably connected to a first side of asymmetric switching pair 110 through first Positive-Channel Metal Oxide Semiconductor (PMOS) device 160 and to a second side of asymmetric switching pair 110 through second PMOS device 170. In addition, third PMOS device 180 is operably connected to signal output 120. Hence, the signal output from signal output 120 is susceptible to fluctuations of first PMOS device 160, second PMOS device 170, and third PMOS device 180 related to process variations, temperature variations, and/or fluctuations of power supply voltage. At least in view of the above, certain rectifier configurations, such as, for example, the configuration illustrated in Figure 1, are not ideally suited to being incorporated into telecommunications devices.

SUMMARY OF THE INVENTION:

[0008] According to certain embodiments of the present invention, a signal strength indicator circuit is provided. The circuit generally includes a signal input for receiving an input signal and a set of rectifiers that normally include an asymmetric switching pair of rectifiers for providing an output signal that is inversely proportional to the input signal, wherein a first side of the asymmetric switching pair is operably connected to a power supply through a resistor. The circuit typically also includes a signal output for outputting the output signal.

[0009] According to certain other embodiments of the present invention, a method of processing a signal entering a signal strength indicator circuit is provided. The method usually includes the steps of receiving an input signal and rectifying the input signal through a set of rectifiers that includes an asymmetric switching pair of rectifiers to generate an output signal that is inversely proportional to the input signal. The method commonly also includes the steps of stabilizing the output signal by operably connecting a first side of the asymmetric switching pair to a power supply through a resistor and outputting the output signal.

[0010] According to yet other embodiments of the present invention, a signal strength indicator circuit is provided. This circuit typically includes receiving means for receiving an input signal and rectifying means for providing an output signal that is inversely proportional to the input signal, the rectifying means usually including an asymmetric switching pair of rectifiers operably connected on a first side thereof to a power supply through a resistor. The circuit also commonly includes outputting means for outputting the output signal.

BRIEF DESCRIPTION OF THE DRAWINGS:

[0011] For a proper understanding of the invention, reference should be made to the accompanying drawings, wherein:

[0012] Figure 1 illustrates a schematic representation of a rectifier configuration according to the related art;

[0013] Figure 2 illustrates a schematic representation of a signal strength indicator circuit that includes rectifiers according to certain embodiments of the present invention;

[0014] Figure 3 illustrates a schematic representation of a rectifier configuration, according to certain embodiments of the present invention, that may be included in the signal strength indicator circuit illustrated in Figure 2;

[0015] Figure 4 illustrates a flowchart that includes the steps of a method of processing a signal received by a signal strength indicator circuit according to certain embodiments of the present invention; and

[0016] Figure 5 illustrates a representative chip on which a Received Signal Strength Indicator (RSSI) circuit according to certain embodiments of the present invention may be included.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS:

[0017] Figure 2 illustrates a schematic representation of a Received Signal Strength Indicator (RSSI) circuit 200 that may be included in telecommunications devices according to certain embodiments of the present invention. In operation, circuit 200 receives signals through input port 210. The signals received at input port 210 are typically AC components of RF signals received by a telecommunication device that includes circuit 200.

[0018] Usually, before reaching input port 210, an AC component has been amplified by an amplifier such as, for example, a Low-Noise Amplifier (LNA) that is operably connected to input port 210. After amplification, the AC component is typically mixed down to an Intermediate Frequency (IF) by

one or more mixers that are operably connected between the amplifier and input port 210.

[0019] As illustrated in Figure 1, circuit 200 may receive both a Q input signal (IN_Q) and an I input signal (IN_I) from an IQ mixer that may be operably connected to input port 210. Generally, the Q input signal and the I input signal are 90° out of phase with each other.

[0020] In Figure 2, input port 210 is operably connected to set of amplifiers 220, which includes three amplifiers, and set of rectifiers 230, which includes five rectifiers. It should be noted that the amplifier closest to input port 210 in set of amplifiers 220 typically receives both the I input signal and the Q input signal and combines these signals before interacting with the other amplifiers in set of amplifiers 220. Hence, instead of providing separate paths for the two received signals, in RSSI circuit 200, both signals are channeled through a single amplification path. This feature of circuit 200 greatly reduces the amount of physical area covered by circuit 200 which, in turn, allows for circuit 200 to be cooled more easily and allows for circuit 200 to utilize less power than RSSI circuits wherein the I input signal and the Q input signal are provided separate paths.

[0021] As shown in Figure 2, two of the rectifiers in set of rectifiers 230 each receive either the I input signal or the Q input signal discussed above directly from an IQ mixer. In contrast, all of the other rectifiers in set of rectifiers 230 receive signals wherein the information previously included in I input signal and Q input signal has been combined. Therefore, in circuit 200, the two rectifiers that receive either the I input signal or the Q input signal draw approximately half of the current as the other rectifiers in set of rectifiers 230.

[0022] Circuit 200 includes capacitor 240 which is operably connected to set of rectifiers 230 and to two resistors 250. Capacitor 240 and resistors 250 make up a resistor-capacitor (RC) filter that filters and smoothes the output port of rectifiers 230 and/or the input to the comparator circuit 260

illustrated in Figure 2, which is operably connected to resistors 250. Resistors 250, as illustrated in Figure 2, are operably connected between set of rectifiers 230 and the power supply (VDD) of circuit 200. The use of resistors 250 to connect to VDD provides additional stability to circuit 200, thereby reducing and/or eliminating the influence of power supply voltage fluctuations on the signal output by the rectifiers in set of rectifiers 230.

[0023] Also included in circuit 200 is comparator circuit 260, which is operably connected to set of rectifiers 230, controller 270, and output port 280. Once the above-discussed I and Q input signals have been combined and processed by set of amplifiers 220 and set of rectifiers 230, a signal is typically forwarded to comparator circuit 260. Comparator circuit 260 then compares the signal it receives with one or more threshold values stored in comparator circuit 260.

[0024] If, for example, the signal it receives exceeds a first threshold value, comparator circuit 260 may determine that the I and Q input signals are too weak to be processed by circuit 200 without losing information. On the other hand, if the received signal is below a second threshold value, comparator circuit 260 may determine that the I and Q input signals are too strong to be processed by circuit 200 without causing circuit saturation. However, if the received signal is between the above-discussed first and second threshold values, comparator circuit 260 may determine that the I and Q input signals are in a range voltage and/or current range that allows for circuit 200 to operate properly.

[0025] When the I and Q signals have been determined to be either too strong or too weak, comparator circuit 260 forwards a signal to output port 280. This signal ultimately causes the gain of the amplifier that led to the I and Q input signals being forwarded from the above-discussed IQ mixer to input port 210 to be switched. On the other hand, if the I and Q input signals are in a range that allows circuit 200 to operate properly, comparator circuit

260 may either forward a signal through output port 280 confirming that no amplifier gain changes need to be made or may not forward any signal at all.

[0026] Controller 270 is typically used to set and/or modify the threshold values stored in comparator circuit 260. Controller 270 may also be used to adjust other variables related to comparator circuit 260.

[0027] Figure 3 illustrates a schematic representation of a rectifier configuration according to certain embodiments of the present invention. The rectifier configuration illustrated in Figure 3 may be used, for example, as any one, any plurality, or all of the rectifiers in set of rectifiers 230 illustrated in Figure 2.

[0028] The rectifier configuration illustrated in Figure 3 includes asymmetric switching pair of rectifiers 300 that is operably connected to signal inputs 310 and signal output 320. According to certain embodiments of the present invention, the asymmetric switching pair of rectifiers 300 is configured to receive an input signal through signal inputs 310 and to provide an output signal through signal output 320 that is inversely proportional to the input signal.

[0029] The rectifier configuration illustrated in Figure 3 may be used, for example, as one of the rectifier in the set of rectifiers 230 in Figure 2 that directly receives either the I input signal or the Q input signal from the above-discussed IQ mixer. The rectifier configuration illustrated in Figure 3 may also be used, for example, as one of the rectifiers in set of rectifiers 230 that receives an input signal from an amplifier in the set of amplifiers 220. In addition, the rectifier configuration illustrated in Figure 3 may be used in other circuits where it would be apparent to those skilled in the art to use such a configuration.

[0030] Operably connected to asymmetric switching pair 300 is biasing circuit 330. How much biasing circuit 330 biases switching pair 300 is dependent on the particulars of the circuit and/or system in which the

rectifier configuration illustrated in Figure 3 is included. However, biasing circuit 330 generally allows for asymmetric switching pair 300 to operate at a current level that is similar to the current level of other circuit/system components.

[0031] As illustrated on the right-hand side of Figure 3, a first side of asymmetric switching pair 300 may be operably connected directly to a power supply (VDD). As illustrated on the left-hand side of Figure 3, particularly when signal output 320 is operably connected to capacitor 240 in Figure 2, signal output 320 may be operably connected to VDD through resistors 250. Hence, in operation, a signal from signal output 320 may then be sent to comparator circuit 260, whose controller 270, as illustrated in Figure 2, provides switching threshold voltages that are also a function of VDD.

[0032] For example, the voltage signal at signal output 320 (V_{OUT_320}) may be equal to $VDD-I_{BIAS\_CIR}R_{250}$, where I_{BIAS_CIR} is a tail current from biasing circuit 330 and R_{250} is the resistance of resistors 250, and the threshold output voltage ($V_{OUT\_THRESHOLD}$) may equal ($VDD-I_{THRESHOLD}R_{290}$), where $I_{THRESHOLD}$ is the threshold current and R_{290} is the resistance of resistors 290. This implies that output signal 320, as well as the right-hand side output of asymmetric switching pair 300 and comparator controller 270, whose configuration, such as the one illustrated in Figure 3, is incorporated into a circuit such as RSSI circuit 200, are all tracking the variation of power supply (VDD) over time. Hence, the signal output from output port 280 is also stabilized.

[0033] Among the reasons that the above-discussed connection allows for relatively stable signals to be output from the rectifier configuration illustrated in Figure 3 is that, as the voltage of the power supply (VDD) fluctuates over time, the rectifier configuration illustrated in Figure 3 also fluctuates in a proportional manner. Hence, power supply voltage is

effectively compensated for and a signal output 320 that is relatively steady over time is capable of being output.

[0034] In the rectifier portion 230 that is illustrated in Figure 2, a set of rectifiers is included. According to certain embodiments of the present invention, all of the rectifier outputs 320 of the rectifiers in the rectifier portion are typically shorted and operably connected to VDD through a resistor.

[0035] The connection of the above-discussed signal output 320 on the left-hand side of Figure 3 to VDD provides signal stability that is additional to the signal stability provided by the connection of the right-hand side of Figure 3 to VDD. More specifically, the connection of the left-hand side of Figure 3 to VDD stabilizes signals output from signal output 320 with respect to process variations. This additional stability may be explained by the fact that, unlike in the rectifier configuration according to the related art illustrated in Figure 1, output signals from the rectifier configuration illustrated in Figure 3 are not influenced by changes in PMOS devices 160, 170, 180 as a function of process variations.

[0036] At least in view of the above, the rectifier configuration illustrated in Figure 3 provides a substantially stable output signal. In addition, when incorporated into a circuit such as, for example, RSSI circuit 200, the rectifier configuration illustrated in Figure 3 improves signal stability in the entire circuit, and in telecommunication devices that include the circuit. Discussed below are representative methods of using the above-discussed rectifier configurations, circuits, and devices discussed herein.

[0100] Figure 4 illustrates a flowchart 400 that includes steps that may be used to process a signal received by a signal strength indicator circuit, such as, for example, RSSI circuit 200, according to certain embodiments of the present invention. Step 410 includes receiving an input signal. The input signal may be received, for example, at input port 210. As shown in Figure 2, the input signal received during step 410 may be received as two or more

portions, such as a first portion from an I signal from a mixer and a second portion as a Q signal from a mixer. When two portions are received from an IQ mixer, the first portion and the second portion may be, for example, 90° out of phase with each other.

[0037] Step 420 includes rectifying the input signal through a set of rectifiers that includes an asymmetric switching pair of rectifiers to generate an output signal that is inversely proportional to the input signal. According to certain embodiments of the present invention, step 420 may be accomplished by incorporating the rectifier configuration illustrated in Figure 3 as one or more of the rectifiers in set of rectifiers 230 in RSSI circuit 200.

[0038] Step 430 includes stabilizing the output signal versus power supply variations by operably connecting a first side of the asymmetric switching pair directly to a power supply. For example, in Figure 3, the right-hand side of asymmetric switching pair 300 is directly connected to VDD.

[0039] Step 440 includes further stabilizing the output signal versus process variations by operably connecting a second side of the asymmetric switching pair to the power supply through a resistor. Step 440 may be implemented by the circuit illustrated in Figure 3, particularly when signal output 320 is operably connected to resistors 250 illustrated in Figure 2.

[0040] Step 450 includes amplifying the input signal through a set of amplifiers that is operably connected to the set of rectifiers. This step may be satisfied by including set of amplifiers 220 illustrated in Figure 2.

[0041] Step 460 includes comparing the output signal to at least one threshold value using a comparator circuit. Step 460 may also include comparing the output signal to at least two threshold values using the comparator circuit. Then, step 470 includes forwarding the output signal.

[0042] When the steps of the above-described method are performed, signals may be received in a signal strength indicator circuit such as, for

example, RSSI circuit 200. The received signals will lead to the creation of stable output signals from circuit 200 and for improved circuit operation.

[0043] Figure 5 illustrates a representative chip 500 on which a Received Signal Strength Indicator (RSSI) circuit according to certain embodiments of the present invention may be included. As illustrated in Figure 5, four low-noise amplifiers (LNAs) 510, 520, 530, 540, each configured to receive telecommunications signals in different frequency ranges, are operably connected to two mixers 550, 560. According to certain embodiments of the present invention, first LNA 510 is a GSM LNA, second LNA 520 is a GSM850 LNA, third LNA 530 is a DCS LNA, and fourth LNA 540 is a PCS LNA. Also, according to certain embodiments first mixer 550 is a GSM/850 mixer to which first and second LNAs 510, 520 are operably connected and second mixer 560 is a DCS/PCS mixer to which third and fourth LNAs 530, 540 are operably connected.

[0044] In chip 500, first and second mixers 550, 560 are operably connected to circuit 570, which may include RSSI circuit 200 illustrated in Figure 2. It should be noted that, in the embodiment of the present invention, the area of chip 500 covered by the LNAs 510, 520, 530, 540, mixers 550, 560 and circuit 570 is greatly reduced, as compared to conventional RSSI or TSSI circuits.

[0045] One having ordinary skill in the art will readily understand that the invention, as discussed above, may be practiced with steps in a different order, and/or with hardware elements in configurations which are different than those which are disclosed. Therefore, although the invention has been described based upon certain preferred embodiments, it would be apparent to those of skill in the art that certain modifications, variations, and alternative constructions would be appropriate, while remaining within the spirit and scope of the invention. In order to determine the metes and bounds of the invention, therefore, reference should be made to the appended claims.